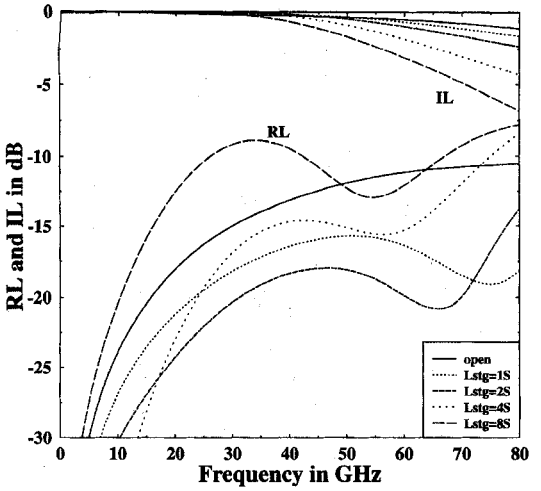

Fig. 4. Return loss and insertion loss of symmetric flip chip CPW with staggered bumps.

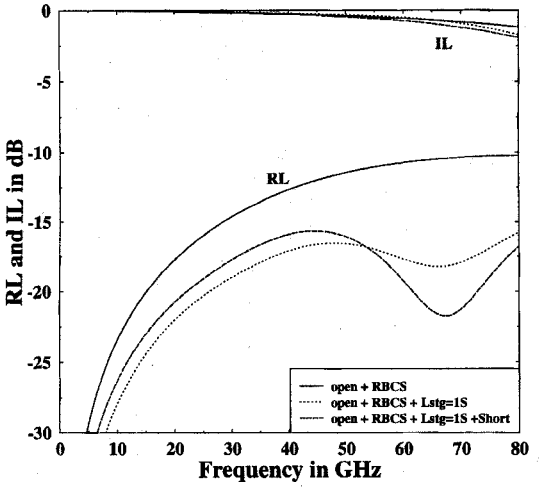

Fig. 5. Return loss and insertion loss of asymmetric flip chip CPW with staggered bumps and short circuit bridge.

including removing one of the ground bumps, or misplacing one of the bumps. In all these cases, the staggered configurations performed better than the in-line bump configurations.

IV. Conclusion

A three-dimensional (3-D) FDTD computer code have been developed to model and investigate the transition between two coplanar waveguides on the chip and the mother board over a wide frequency range. Our results includes three different CPW transitions. These are open, staggered and short circuit bridge. Using these models, we investigated the effects of the bump discontinuity and the structure asymmetry on the performance of a flip chip CPW package. The results indicate that a reduction of the bump reflection can be obtained using the staggered bumps and the short circuit bridge designs. A reduction in the bump reflection of up to 8 dB is achieved over a wide frequency range. However, the insertion loss improvement may not be very significant. The effect of structure asymmetry has been studied. The deterioration of the package performance due to asymmetry can be significantly reduced by incorporating one of the above designs.

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Thermal Management for High-Power Active Amplifier Arrays

Nicholas J. Kolias and Richard C. Compton

***Abstract*—Much of the active array work reported to date has been directed toward the demonstration of prototypes at low-power levels. Analysis results presented here show that overheating failures will occur as these arrays are scaled to reasonable output powers. Large air-cooled heat sinks attached to the backside of a thinned array can be used for single-sided designs such as oscillator arrays, but heat sinking becomes substantially more difficult for two-sided transmission-type arrays. For these designs, a possible solution is described which uses an aluminum-nitride dielectric layer to facilitate conduction to heat sinks on the array's perimeter.**

I. Introduction

Quasi-optical active arrays provide a means of combining the outputs of large number of semiconductor devices [1]–[8]. Such arrays could provide an alternative to tubes for high power millimeter

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TABLE I
CALCULATED SURFACE TEMPERATURE OF THE ARRAY WITH NO HEAT SINKING

Array Size	Air speed (ft/min)	h_r (W/(°C·m²))	h_c (W/(°C·m²))	T_s (°C)
3.56" sq.	0	39.7	12.0	485
	500	35.0	19.7	447
	1000	30.8	27.9	409
1.89" sq.	0	95.7	16.0	797
	500	87.4	27.1	761
	1000	79.7	38.3	725

wave applications. Despite the amount of work done on quasi-optical arrays over the past few years, an important aspect of the designs, thermal analysis, has largely been neglected. Because of the inherently low device efficiencies, considerable heat is generated by a practical array. Thermal management must be accommodated early in the array design process, as he required heat sinking may seriously impact the electromagnetic performance of the array.

The maximum amount of heat which a CW array will generate occurs when the rf input signal is interrupted, as all the dc input power (P_{dc}) is converted to heat. This maximum heat may be calculated from $P_{heat} = P_{out}(1 - 1/G)/\eta_{pae}$ where G is the array gain, P_{out} is the array's RF output power, and η_{pae} is the array power-added efficiency. For a typical array at 35 GHz, $P_{out} = 100$ W, $G = 7.5$ dB, $\eta_{pae} = 25$,% and $P_{heat} = 329$ W [9]–[11]. Even with devices which operate at the theoretical maximum class A efficiency of 50%, the maximum total array heat generation is still approximately 165 W. This heat leads to a temperature rise of the array's transistor junctions, which, for reliable operation, need to be kept below their specified maximum temperature, typically 150°C. In the next section, analysis is presented which shows that forced air cooling across the array is inadequate. In Section III, a cooling approach in which the array is mounted on a thick aluminum-nitride (AlN) dielectric is described.

II. CALCULATED SURFACE TEMPERATURE OF THE ARRAY

A. Array with No Heat Sinking

For a simple array the heat, P_{heat}, can be removed via thermal radiation or natural convection from the front and back surfaces. Assuming that the heat is generated uniformly across the array, the surface temperature T_s is given by [12], [13]

$$T_s = T_{amb} + \left[\frac{1}{(\epsilon h_r + h_c)A}\right] P_{heat} \tag{1}$$

where T_{amb} is the ambient temperature, A is the total array surface area, ϵ is the surface emissivity, and h_r and h_c are the radiation and convection transfer coefficients, respectively. Both h_r and h_c are temperature dependent, while h_c is also geometry dependent. Table I gives some typical surface temperatures for arrays assuming $P_{heat} = 329$ W, $T_{amb} = 25$°C, and $\epsilon = 0.8$. The array temperature can be reduced slightly with forced convection, which has the effect of increasing h_c (see Table I) [12], [13]. These results neglect an additional junction temperatures rise due to "heat spreading" from the discrete devices. Thus, the actual junction temperature would be even higher. Clearly, radiation and air convection from the array surfaces alone cannot successfully cool the array.

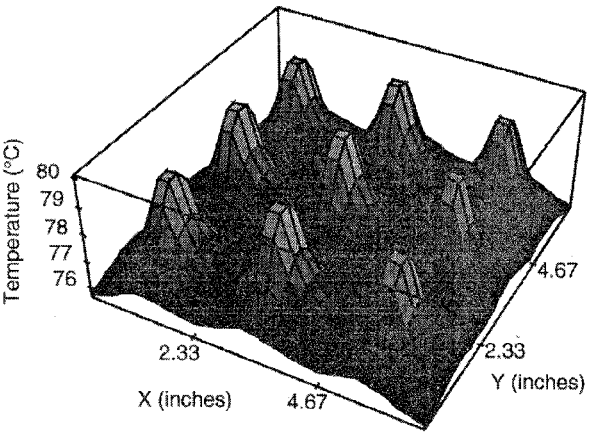

Fig. 1. Output of modeling program for a 3×3 array of power resistors, each dissipating 4W, mounted on a $7''$ square, 40 mil thick, piece of aluminum.

B. Array with Backside Heat Sinking

Some arrays such as oscillator arrays require electromagnetic access on only one side of the array. These arrays can be adequately cooled by mounting a thinned array onto a large, heat sink using standard MMIC methods. However in most quasi-optical amplifier designs, in which one side of the array is used for free-space input and the other side for output, a large metal heat sink cannot be placed on the backside. Heat sinks may be placed around the perimeter of these transmission arrays. A finite-difference three-dimensional (FD3D) thermal modeling program was developed to calculate the thermal distribution when a heat sink is placed at the perimeter of an array. The program was verified by testing a variety of analytically solvable problems. Results of the program were also checked for a $7''$ square aluminum plate containing a three-by-three array of power resistors each dissipating 4W. The output of the program (shown in Fig. 1) predicts a peak temperature of 80°C for the array, which is within 5°C of the temperature measured using thermocouples. This small difference could easily be attributed to uncertainty in the values of ϵ and h_c.

The FD3D program was used to analyze a $t = 25$ mil thick, $1.89''$ square GaAs array heat sunk on two opposite edges; the temperature rise at the middle of the array was found to be exceedingly large (≈697°C above ambient) for a power dissipation of 329 W. This compares well with the approximate relation for the temperature rise above ambient given by [12], [15]

$$T_{rise} \approx \frac{Q_{tot}}{2hab}\left\{1 - \frac{1}{\cos h\left[0.707a\sqrt{h/(kt)}\right]}\right\} = 672°\text{C} \tag{2}$$

where Q_{tot} is the total array heat dissipation (= 329 W), k is the thermal conductivity of GaAs (≈50 W/m°C), $a = 1.89''$ is the distance between the opposite heat sinks, $ab = 1.89''$ square is the array area, and $h = h_c + \epsilon h_r$ (assumed constant across the array) = 60 W/(m² · °C). With heat sinks on all four edges, simulations show that the peak array temperature is 508°C, which is still much higher than the 150°C maximum. Thus, the thin nature of transmission amplifier arrays leads to large temperature gradients as the heat conducts to the array edges.

III. CONDUCTION COOLING THE ARRAY BY USING A DIELECTRIC SLAB

Simulations show, however, that if the GaAs is thinned down and mounted on a dielectric slab (that is heat-sunk on the edges)

TABLE II
DIELECTRIC MATERIALS WITH HIGH THERMAL CONDUCTIVITY (k)

Material	ε_r	tan δ (10 GHz)	k (W/(m·°C)) (Room Temp)	Disadvantages
Diamond	5.6	< 0.002	> 1000	Expensive
SiC	9.7		500	Not readily available
BeO	6.5	≤ 0.004	260	Toxic dust
AlN	8.5	0.0039	170	—

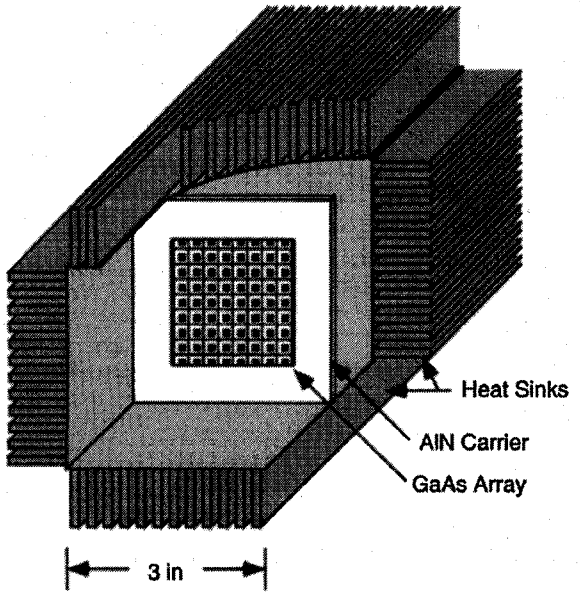

Fig. 2. Cut-open view of the geometry used in simulations for conduction coding of the array using an AlN slab.

with significantly higher thermal conductivity, the temperature rise can be reduced to well below the 150°C maximum. Some possible dielectric materials for accomplishing this task are listed in Table II. Of these materials, diamond is expensive and BeO is highly toxic. SiC technology, while showing much promise for microwave power applications, is currently not yet readily available [14]. AlN, while having slightly lower thermal conductivity than SiC, has none of these other disadvantages.

The 329 W, 1.89″ square array may be cooled by mounting it on a 3″ square AlN substrate placed inside of a square metal tube which has heat sinks attached to its outer sides (Fig. 2). By contacting the AlN on all four sides, the metal tube effectively edge-sinks the array. Simulations done for this geometry show that the temperature rise from the edge of the AlN to the middle point on the array (T_{AlN}) is 111°C for AlN of thickness 3 mm, and 68° for AlN of thickness 5 mm. These numbers assume uniform array heat dissipation. Convection and radiation are neglected because these effects may be limited in practice by the presence of quarter-wave matching layers. To obtain the actual maximum junction temperature (T_j) for this design, this temperature rise in the AlN (T_{AlN}) needs to be added to the temperature rise of the heat sink (T_{sa}) and the temperature rise due to the thermal resistance between the transistor hot-spot and the bottom of the GaAs substrate (θ_{jc}). In addition, the temperature rises due to the thermal contact resistance between the GaAs and the AlN dielectric (θ_{cd}), the thermal contact resistance between the AlN and the heat sink (θ_{ds-c}), and the thermal "spreading" resistance from the AlN edge to the cold heat sink (θ_{ds-s}) need to be accounted for, yielding [15]

$$T_j - T_{amb} = \theta_{jc}Q_i + \theta_{cd}Q_{tot} + \theta_{ds-c}\left(\frac{Q_{tot}}{4}\right) + \theta_{ds-s}\left(\frac{Q_{tot}}{4}\right) + T_{AlN} + T_{sa} \quad (3)$$

where Q_i is the individual device heat dissipation and Q_{tot} is the total array heat dissipation.

Use of a nonconducting thermal epoxy (so as to not reflect the incident beam) such as Thermalloy's Thermalbond (k = 1.35 W/m°C) results in a $\theta_{cd} = L/(kA)$ of 0.016°C/W and a corresponding temperature rise of 5.3°C for $L = 50$ μm of epoxy thickness. At the contact between the edge of the AlN and the heat sink, a higher conductivity, silver loaded epoxy ($k = 4$ W/m°C) can be used. This choice gives a θ_{ds-c} of 0.0328°C/W and a temperature rise of 2.7°C for 5 mm thick AlN and 50 μm of epoxy thickness. The spreading resistance at the AlN edge, θ_{ds-s}, which accounts for the nonuniform temperature distribution on the heat-sink, can be estimated using Mikic's relation for spreading from a long, strip heat source [15], [16]

$$\theta_{ds-s} = \frac{1}{\pi Lk}\ln\left[\frac{1}{\sin\left(\frac{\pi a}{2b}\right)}\right] \approx 0.076 \quad (4)$$

where L is the length of the heat source (3 in), k is the thermal conductivity of the heat sink 200 W/m°C for Aluminum), $2a$ is the width of the heat source (= 5 mm), and $2b$ is the length of the heat sink (taken to be 12 in). These values result in a temperature rise of 6.3°C. Devices with θ_{jc}'s of less than 50°C/W can be obtained by thinning down the GaAs and spacing out the transistor fingers (in well-spaced multi-finger designs, thermal resistances in the 30's have been achieved for 44 GHz devices [17]). For an 1000 element array with each device dissipating 329 mW, a θ_{jc} of 50°C/W results in an additional temperature rise of 16.5°C.

Entering these values into (3) gives a maximum junction temperature above ambient of $T_j - T_{amb} = 98.7°\text{C} + T_{sa}$. For an ambient temperature of 25°C, keeping the temperature below 150°C requires the total heat sink temperature rise to be less than 26.2°. This is difficult to do with natural convection unless one uses very large, custom-made heat sinks. With forced convection, however, it can be done using standard extrusions from a heat-sink manufacturer. Thus, by using a 5 mm thick AlN substrate to transport the 329 W of heat, the transmission array can be cooled successfully. The above calculated junction temperature rise is a worst-case result, as it neglects any convection or radiation heat loss from the array, AlN, or matching-layer surfaces. In practice a thicker AlN slab could be used to allow a larger safety margin.

The surface temperature distribution or the array of this example has been calculated via computer simulation and is plotted in Fig. 3. These results show that the end devices of the array heat up to ≈60°C above the heat-sink surface temperature, while the middle devices are at 98.7°C above. Simulations have also been done which solve (3) as a function of Q_{tot} for various AlN thickness. These results, which are plotted in Fig. 4, assume that each array device has a θ_{jc} of 50°C/W and is dissipating a Q_i of Q_{tot}/1000 W. In addition, the array adhesives are assumed to have conductivities and thicknesses as in the above example, and the array is assumed to be 1.89″ square mounted on a 3″ square AlN substrate. Using this graph, the junction temperature rise above the sink surface temperature, $T_j - T_{amb} - T_{sa}$, can be calculated for the array when it dissipates different amounts

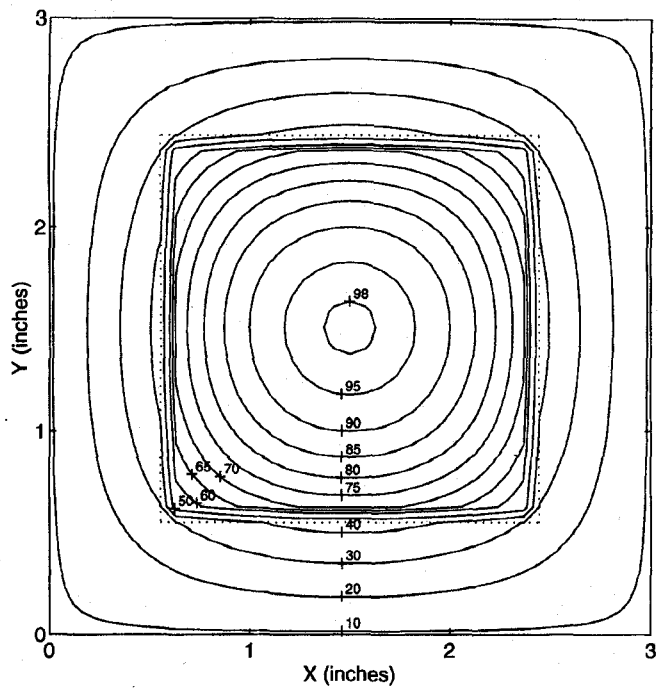

Fig. 3. Contour plot of the array junction temperature distribution (in °C for a 329 W, 1.89″ square array (dotted line) mounted on a 3″ square AlN dielectric. The plotted temperature is the temperature rise above the sink surface temperature ($= T_j - T_{sa} - T_{amb}$).

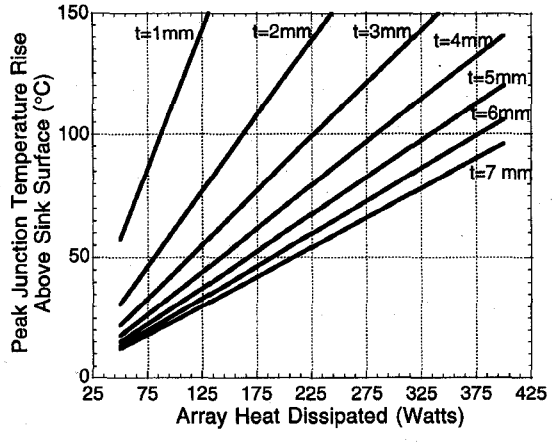

Fig. 4. Peak junction temperature above sink surface temperature versus total power dissipated for AlN substrates of various thicknesses, t.

of heat or when different thicknesses of AlN are used. From this plot, one can see that for arrays which dissipate less than 100 W, an AlN thickness of 2 mm is needed, while for arrays which dissipate 400 W, the AlN must be at least 7 mm thick.

The addition of the AlN slab may affect the electromagnetic performance of the array, as the dielectric slab, as well as the metal heat sinks on the dielectric edges, could reflect significant portions of the incident beam. To minimize these reflections, the dielectric slab should be made longer and wider than the array, and quarter-wave anti-reflection layers can be placed on the surface of the dielectric. The feasibility of using matching layers was tested out by surrounding the array in [6] on both sides with alumina slabs followed by quarter-wave anti-reflection dielectric layers of $\varepsilon_r = 3.27$. The array yielded very similar results (with $\approx$1.5 dB of additional loss and 1.5 GHz less bandwidth) to those presented in [6].

IV. Conclusion

The heat generated in a typical high-power, quasi-optical amplifier array design has been examined, and found to be problematically large, in excess of 300 W. Analysis shows that dissipating this heat without raising the transistor junction temperature above a 150°C maximum cannot be done by simple natural convection or by forced air convection from the array surfaces alone. Large, air-cooled heat sinks attached to the backside of a thinned array can successfully be used for reflection-type amplifier designs, but most all of the currently proposed designs are transmission-type. For transmission-type designs, a possible solution has been proposed which uses an AlN layer to transport the array heat to a large, air-cooled heat sink.

Acknowledgment

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